Most Frequently Occurring Classifications of Patents Returned
From A Search of 10073830 on June 30, 2004

Original Classifications
 11 714/727
  6 714/726
  3 324/158.1
  3 714/724
  2 324/763
  2 326/38
  2 703/14
  2 714/731
  2 714/733
  2 717/139

Cross-Reference Classifications
  9 714/727
  7 714/724
  4 714/30
  4 714/731
  4 714/733
  3 324/158.1
  3 714/725
  3 714/726
  3 716/4
  2 326/40
  2 326/41
  2 326/46
  2 703/13
  2 714/42
  2 714/734
  2 716/1
  2 716/16
  2 716/17

Combined Classifications
 20 714/727
 10 714/724
  9 714/726
  6 324/158.1
  6 714/731
  6 714/733
  5 714/30
  3 326/38
  3 703/14
  3 714/725
  3 716/16

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3   716/4
2   324/763
2   326/39
2   326/40
2   326/41
2   326/46
2   327/202
2   365/201
2   703/13
2   714/42
2   714/734
2   716/1
2   716/17
2   717/139
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Titles of Most Frequently Occurring Classifications of Patents Returned

From A Search of 10073830 on June 30, 2004


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 20  714/727        (11 OR, 9 XR)
           Class    714 :  ERROR DETECTION/CORRECTION AND FAULT
                              DETECTION/RECOVERY
           714/699          PULSE OR DATA ERROR HANDLING
           714/724          .Digital logic testing
           714/726          ..Scan path testing (e.g., level sensitive scan
                              design (LSSD))
           714/727          ...Boundary scan


 10  714/724        (3 OR, 7 XR)
           Class    714 :  ERROR DETECTION/CORRECTION AND FAULT
                              DETECTION/RECOVERY
           714/699          PULSE OR DATA ERROR HANDLING
           714/724          .Digital logic testing


  9  714/726        (6 OR, 3 XR)
           Class    714 :  ERROR DETECTION/CORRECTION AND FAULT
                              DETECTION/RECOVERY
           714/699          PULSE OR DATA ERROR HANDLING
           714/724          .Digital logic testing
           714/726          ..Scan path testing (e.g., level sensitive scan
                              design (LSSD))


  6  324/158.1      (3 OR, 3 XR)
           Class    324 :  ELECTRICITY:  MEASURING AND TESTING
           324/158.1        MISCELLANEOUS


  6  714/731        (2 OR, 4 XR)
           Class    714 :  ERROR DETECTION/CORRECTION AND FAULT
                              DETECTION/RECOVERY
           714/699          PULSE OR DATA ERROR HANDLING
           714/724          .Digital logic testing
           714/726          ..Scan path testing (e.g., level sensitive scan
                              design (LSSD))
           714/731          ...Clock or synchronization


  6  714/733        (2 OR, 4 XR)
           Class    714 :  ERROR DETECTION/CORRECTION AND FAULT
                              DETECTION/RECOVERY
           714/699          PULSE OR DATA ERROR HANDLING
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        714/724         .Digital logic testing
        714/733         ..Built-in testing circuit (BILBO)

  5  714/30          (1 OR, 4 XR)
        Class    714 :  ERROR DETECTION/CORRECTION AND FAULT
                           DETECTION/RECOVERY
        714/100         DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING

        714/1           .Reliability and availability
        714/25          ..Fault locating (i.e., diagnosis or testing)

        714/27          ...Particular access structure
        714/30          ....Built-in hardware for diagnosing or testin
g
                           within-system component (e.g., microprocess
or test mode
                           circuit, scan path)

  3  326/38          (2 OR, 1 XR)
        Class    326 :  ELECTRONIC DIGITAL LOGIC CIRCUITRY
        326/37          MULTIFUNCTIONAL OR PROGRAMMABLE (E.G.,
                           UNIVERSAL, ETC.)
        326/38          .Having details of setting or programming of
                           interconnections or logic functions

  3  703/14          (2 OR, 1 XR)
        Class    703 :  DATA PROCESSING:  STRUCTURAL DESIGN,
                           MODELING, SIMULATION, AND EMULATION
        703/13          SIMULATING ELECTRONIC DEVICE OR ELECTRICAL
                           SYSTEM
        703/14          .Circuit simulation

  3  714/725         (0 OR, 3 XR)
        Class    714 :  ERROR DETECTION/CORRECTION AND FAULT
                           DETECTION/RECOVERY
        714/699         PULSE OR DATA ERROR HANDLING
        714/724         .Digital logic testing
        714/725         ..Programmable logic array (PLA) testing

  3  716/16          (1 OR, 2 XR)
        Class    716 :  DATA PROCESSING:  DESIGN AND ANALYSIS OF
                           CIRCUIT OR SEMICONDUCTOR MASK
        716/1           CIRCUIT DESIGN
        716/12          .Routing (e.g., routing map, netlisting)
        716/16          ..PLA, PLD, FPGA, OR MCM

  3  716/4           (0 OR, 3 XR)
        Class    716 :  DATA PROCESSING:  DESIGN AND ANALYSIS OF
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              CIRCUIT OR SEMICONDUCTOR MASK
     716/1         CIRCUIT DESIGN
     716/4         .Testing or evaluating


2  324/763      (2 OR, 0 XR)
     Class   324 :  ELECTRICITY:  MEASURING AND TESTING
     324/500         FAULT DETECTING IN ELECTRIC CIRCUITS AND OF
                         ELECTRIC COMPONENTS
     324/537         .Of individual circuit component or element
     324/763         ..DUT including test circuit


2  326/39       (1 OR, 1 XR)
     Class   326 :  ELECTRONIC DIGITAL LOGIC CIRCUITRY
     326/37          MULTIFUNCTIONAL OR PROGRAMMABLE (E.G.,
                         UNIVERSAL, ETC.)
     326/39          .Array (e.g., PLA, PAL, PLD, etc.)


2  326/40       (0 OR, 2 XR)
     Class   326 :  ELECTRONIC DIGITAL LOGIC CIRCUITRY
     326/37          MULTIFUNCTIONAL OR PROGRAMMABLE (E.G.,
                         UNIVERSAL, ETC.)
     326/39          .Array (e.g., PLA, PAL, PLD, etc.)
     326/40          ..With flip-flop or sequential device


2  326/41       (0 OR, 2 XR)
     Class   326 :  ELECTRONIC DIGITAL LOGIC CIRCUITRY
     326/37          MULTIFUNCTIONAL OR PROGRAMMABLE (E.G.,
                         UNIVERSAL, ETC.)
     326/39          .Array (e.g., PLA, PAL, PLD, etc.)
     326/41          ..Significant integrated structure, layout, or
                         layout interconnections


2  326/46       (0 OR, 2 XR)
     Class   326 :  ELECTRONIC DIGITAL LOGIC CIRCUITRY
     326/37          MULTIFUNCTIONAL OR PROGRAMMABLE (E.G.,
                         UNIVERSAL, ETC.)
     326/46          .Sequential (i.e., finite state machine) or
                         with flip-flop


2  327/202      (1 OR, 1 XR)
     Class   327 :  MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR
                         DEVICES, CIRCUITS, AND SYSTEMS
     327/100         SIGNAL CONVERTING, SHAPING, OR GENERATING
     327/185         .Particular stable state circuit (e.g.,
                         tristable, etc.)
     327/199         ..Circuit having only two stable states (i.e.,
                         bistable)
     327/202         ...Master-slave bistable latch
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2 365/201   (1 OR, 1 XR)
     Class   365 : STATIC INFORMATION STORAGE AND RETRIEVAL
     365/189.01   READ/WRITE CIRCUIT
     365/201   .Testing

2 703/13   (0 OR, 2 XR)
     Class   703 : DATA PROCESSING: STRUCTURAL DESIGN,
                      MODELING, SIMULATION, AND EMULATION
     703/13   SIMULATING ELECTRONIC DEVICE OR ELECTRICAL
                    SYSTEM

2 714/42   (0 OR, 2 XR)
     Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                      DETECTION/RECOVERY
     714/100   DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING

     714/1   .Reliability and availability
     714/25   ..Fault locating (i.e., diagnosis or testing)

     714/40   ...Component dependent technique
     714/42   ....Memory or storage device component fault

2 714/734   (0 OR, 2 XR)
     Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                      DETECTION/RECOVERY
     714/699   PULSE OR DATA ERROR HANDLING
     714/724   .Digital logic testing
     714/734   ..Structural (in-circuit test)

2 716/1   (0 OR, 2 XR)
     Class   716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
                      CIRCUIT OR SEMICONDUCTOR MASK
     716/1   CIRCUIT DESIGN

2 716/17   (0 OR, 2 XR)
     Class   716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
                      CIRCUIT OR SEMICONDUCTOR MASK
     716/1   CIRCUIT DESIGN
     716/17   .Programmable integrated circuit (e.g., basic
                    cell, standard cell, macrocell)

2 717/139   (2 OR, 0 XR)
     Class   717 : DATA PROCESSING: SOFTWARE DEVELOPMENT,
                      INSTALLATION, AND MANAGEMENT
     717/100   SOFTWARE PROGRAM DEVELOPMENT TOOL (E.G.,
                      INTEGRATED CASE TOOL OR STAND-ALONE DEVEL
OPMENT TOOL)

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PLUS Search Results for S/N 10073830, Searched June 30, 2004

The Patent Linguistics Utility System (PLUS) is a USPTO automated sear
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system for U.S. Patents from 1971 to the present. PLUS is a
query-by-example search system which produces a list of patents that a
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most closely related linguistically to the application searched. This
search was prepared by the staff of the Scientific and Technical
Information Center, SIRA.

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